

## **REMARKS**

The Office Action dated December 16, 2004, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 1-6 and 8-10 have been amended. Applicants submit that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1-10 are pending in the present application and claims 1-10 are respectfully submitted for consideration.

### **Formal Matters**

Claims 1-10 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite because the Examiner appears to be unclear about the subject matter recited in the claims.

The claims have been amended responsive to the rejection. Furthermore, Applicant highlights Figures 4 and 8 of the drawings along with pages 12-14 and 19-20 of the Specification. It is submitted that at least the above highlighted sections of the present application clearly disclose the subject matter of the present invention, and therefore the subject matter recited in claims 1-10 is definite. Hence, Applicant respectfully requests withdrawal of the rejection.

### **Claims 1-10 Rejected under 35 U.S.C. § 103 (a)**

Claims 1-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Dhong et al. (U.S. Patent No. 6,014,763, hereinafter "Dhong") in view of Whetsel (U.S. Patent No. 6,405,335). Applicant respectfully submits that each of claims 1-10

recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claims 1, 5 and 9 each recites an integrated circuit device comprising, among other features, a plurality of boundary scan registers, serially connected to constitute a shift register, for inputting and outputting scan-in data or scan-out data, the scan-in data being input to the shift register and the scan-out data being output from the shift register, wherein each of the boundary scan registers selectively input an input data including one of an output of the input buffer and the scan-in or scan-out data, holds the input data, and selectively output either the input data or an output from one of the serial to parallel conversion circuits.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicant's invention.

Dhong discloses a method of scanning an integrated circuit, by converting a parallel scan input (scan data and scan control) to serial, passing the serial scan input through scan circuitry to create a serial scan output, converting the scan output from serial to parallel, transmitting the scan output in parallel from the integrated circuit to the tester. Dhong further provides a tester clock signal that is derived by synchronizing the tester to a divided clock signal ( $1/N$ ) of the integrated circuit. Communications take place at a speed of the tester clock signal, but the scan operates at the full operational speed of the device under test.

Whetsel discloses an integrated circuit comprising core circuitry including functional inputs and functional outputs, an input pad and an output pad. Whetsel also provides a scan distributor circuitry connected between the input pad and, selectively, at least some of the functional inputs, through a multiplexer. Scan collector circuitry

connects selectively between at least some of the functional outputs and the output pad, through a demultiplexer. A strobe is inputted to a series of buffers 2208, 2210, 2212, and 2214 connected such that the output of the first buffer drives scan path 1 and the input of the second buffer, the second buffer drives the input of scan path 2 and the input of the third buffer, and so on until the last buffer drives only the last scan path.

Applicant respectfully submits that each of claims 1, 5 and 9 recites subject matter that is neither disclosed nor suggested by the cited prior art. In particular, neither Dhong nor Whetsel, taken together or in combination, disclose or suggest at least the limitation of “a plurality of boundary scan registers, serially connected to constitute a shift register, for inputting and outputting scan-in data or scan-out data, the scan-in data being input to the shift register and the scan-out data being output from the shift register, wherein each of the boundary scan registers selectively input an input data including one of an output of the input buffer and the scan-in or scan-out data, holds the input data, and selectively output either the input data or an output from one of the serial to parallel conversion circuits.”

As characterized by the Office Action, Dhong uses the steps of transmitting a scan input in parallel from a tester to the integrated circuit, converting the scan input at the integrated circuit from parallel to serial, and passing the serial scan input through scan circuitry of the integrated circuit to create a serial scan output. The Office Action further characterizes Whetsel as teaching an integrated circuit for testing in which the input signal is input to a series of input buffers connected to the individual scan paths (column 28, lines 45-61). However, Applicant submits that Office Action failed to indicate at least the limiting feature of “a plurality of boundary scan registers, serially

connected to constitute a shift register, for inputting and outputting scan-in data or scan-out data, the scan-in data being input to the shift register and the scan-out data being output from the shift register, wherein each of the boundary scan registers selectively input an input data including one of an output of the input buffer and the scan-in or scan-out data, holds the input data, and selectively output either the input data or an output from one of the serial to parallel conversion circuits” in the cited prior art. Therefore, Applicant respectfully submits that claims 1, 5 and 9 are allowable.

To establish *prima facie* obviousness, each feature of a rejected claim must be taught or suggested by the applied art of record. See M.P.E.P. §2143.03 and *In re Royka*, 490 F.2d 981 (CCPA 1974). As explained above, Dhong and Whetsel, alone or in combination, do not teach or suggest each feature recited by pending Claims 1, 5 and 9. Accordingly, for the above provided reasons, Applicants respectfully submit that pending Claims 1, 5 and 9 are not rendered obvious under 35 U.S.C. § 103 by Dhong and Whetsel.

As claims 2-4 depend from claim 1, claims 6-8 depend from claim 5, and claim 10 depends from claim 9, Applicant respectfully submit that claims 2-4, 6-8 and 10 should be deemed allowable for at least the same reasons claims 1, 5 and 9 are allowable, as well as for the additional subject matter recited therein.

Therefore, Applicants respectfully request withdrawal of the rejection.

### **Conclusion**

In view of the above, Applicants respectfully submit that each of claims 1-10 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the

claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1-10 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300 referencing Attorney Docket No. 108066-00037.

Respectfully submitted,



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Enclosures: RCE Transmittal  
Petition for Extension of Time (2 Month)